REMARKS

The above amendments to the above-captioned application along with the following remarks are being submitted as a full and complete response to the Office Action dated January 22, 2008. In view of the above amendments and the following remarks, the Examiner is respectfully requested to give due reconsideration to this application, to indicate the allowability of the claims, and to pass this case to issue.

Status of the Claims

Claims 1-24 and 29-31 are under consideration in this application. Claims 1, 13 and 29 being amended, as set forth above and in the attached marked-up presentation of the claim amendments, in order to more particularly define and distinctly claim Applicants' invention. New claims 30-31 are being added. All the amendments to the claims are supported by the specification. Applicants hereby submit that no new matter is being introduced into the application through the submission of this response.

Formality Rejection

Claim 1 was rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. As indicated, the claims are being amended as required by the Examiner. Accordingly, the withdrawal of the outstanding informality rejection is in order, and is therefore respectfully solicited.

Prior Art Rejections

Under 35 U.S.C. §103(a), the Examiner rejected: (1) Claims 1-4, 6-7, 9, 12-15, 17-18, 20, 23-24 and 29 as being unpatentable over US Publication No. 2003/0067424 to Akimoto et al. in view of newly cited US Patent No. 7,167,169 to Libsch. (2) Claims 5, 8, 16 and 19 as being unpatentable over Akimoto '424 in view of Libsch '169, and further in view of US Patent No. 5,250,931 to Misawa et al. (3) Claims 10 and 21 as being unpatentable over Akimoto '424 in view of Libsch '169, and further in view of US Patent No. 6,670,936 to Akimoto et al.; and (4) Claims 11 and 22 as being unpatentable over Akimoto '424 in view of Libsch '169, and further in view of US Patent No. 6,812,912 to Miyajima et al.. These rejections have been carefully considered, but are most respectfully traversed.

The image display device of the present invention (for example, the embodiment depicted in Figs. 1-4), as now recited in claim 1, comprises: a display part 20 configured by a plurality of pixels 10 each having an electro-luminescent element 1 driven to illuminate

according to a display signal voltage Vs; a signal line 8 used to write said display signal voltage Vs in said pixel 10 (during a "writing period", 1st half of a frame in Fig. 3 with the ting details shown in Fig. 4); a pixel selector 15 for selecting a pixel from said plurality of pixels so as to write said display signal voltage Vs therein through said signal line 8; a display signal voltage generator 16 for generating said display signal voltage Vs; an illuminating state controller for controlling a selection of an illuminating state or a non-illuminating state for each of said plurality of pixels at a time; and a constant voltage supply for supplying a constant voltage Vil to each of said plurality of pixels through said signal line 8 when said illuminating state is selected for said selected pixel. One end of said electro-luminescent element 1 provided in each said pixel 10 is connected to a common power supply while the other end of said electro-luminescent element 1 is selectively connected to a first source/drain electrode of an electro-luminescent element driving transistor 2 through a first switch 7, said transistor 2 has a threshold voltage Vth, a second source/drain electrode of said electro-luminescent element driving transistor 2 is connected to a power supply line 9 applied with a prescribed voltage (from a power input line 13 in Fig. 1), and the gate of said electro-luminescent element driving transistor 2 is connected to the signal line 8 through a capacitance 4 and selectively connected to the first source/drain electrode of said electro-luminescent element driving transistor 2 through a second switch 6 (claim 2; Fig. 2). When said illuminating state is selected (during a "illuminating period", 2nd half of the frame in Fig. 3), the first switch 7 is fixed as ON, the second switch 6 is fixed as OFF, and the constant voltage Vil lower than display signal voltage Vs is applied to the signal line 8 (Fig. 1; "*the signal line switch 17 switches the signal line 8 between the signal voltage generation circuit 16 and the constant voltage input line 14*" p. 10, lines 1-4) such that a voltage that is lower than said prescribed voltage (e.g., by (Vs-Vil+ |Vth|); claim 29) appears at the gate of said transistor 2 (Fig. 3; p. 13, lines 19-25; p. 14, lines 5-11).

Applicants contend that none of the cited prior art references teaches or suggests "supplying a constant voltage Vil to each of said plurality of pixels through said signal line 8 when said illuminating state is selected for said selected pixel," that "When said illuminating state is selected, the first switch 7 is fixed as ON, the second switch 6 is fixed as OFF, and the constant voltage Vil lower than display signal voltage Vs is applied to the signal line 8 such that a voltage that is lower than said prescribed voltage appears at the gate of said transistor 2" as according to the invention.

As recited in claim 13, one end of the signal line 8 is connected to the display signal voltage generator 16 and a constant voltage generator ("*constant voltage supplying means for*

supplying a constant voltage to each pixel through a signal line" p. 5, lines 24-25; "*the signal line switch 17 switches the signal line 8 between the signal voltage generation circuit 16 and the constant voltage input line 14*" p. 10, lines 1-4) through a third switch 17 (Fig. 1).

In claim 30, when said illuminating state is selected, said electro-luminescent element is driven to by a voltage of (Vs-Vil) to illuminate. In claim 31, the constant voltage Vil applied to the signal line is the lowest level of said display signal voltage Vs (Figs. 3-4; Fig. 4 shows the details of the writing period of Fig. 3, to connect the two figures, Vil = lowest level of Vs).

As admitted by the Examiner (p. 4, 2nd to last paragraph of the outstanding Office Action), Akimoto does not disclose supplying a **constant** voltage to each pixel during the **illuminating** state or that the constant voltage is lower than the common supply voltage. As pointed out by the Examiner, "*Akimoto further discloses, a constant voltage supply, as evidenced by the signal line data during the write period in figure three. During an illumination period, Akimoto supplies a triangular signal amplitude as seen in figure three*" (p. 4, 3rd to last paragraph of the outstanding Office Action).

Libsch was relied upon by the Examiner to provide such teachings. In particular, the Examiner (p. 6, last paragraph of the outstanding Office Action) asserted that an image display device having an electro-luminescent element pixel circuit (42 in Fig. 2a), wherein a constant voltage supply (64, 62 in Fig. 2a) provides a constant voltage to the pixel through a signal line (48 in Fig. 2a) when said illuminating state is selected for said selected pixel (col. 3, lines 32-34).

Indeed, V5 is a display signal voltage being written by a signal line (col. 8, line 31-32), and Libsch applies V5 to the drain of the data transfer transistor Q 1 (col. 8, lines 31-32) during the (2) mode of operation OLED illumination during times 0.1 msec and 0.2 msec (col. 8, lines 39-40; Fig. 5F). However, V5 changes constantly to indicate data written rather than always maintaining at a constant value. Besides, only one rewriting data is indicated in Fig. 5E, this is because Fig. 5E shows a simulation data being written to a pixel, that is, the concept of a constant voltage is applied to the signal line via a switch 17 (claim 13) during the ILLUMINATE period is not exist in Libsch.

Regarding claim 13, Akimoto (p. 7, 5th to 6th paragraphs of the outstanding Office Action) only uses a signal select line to alternate a signal input switch 23 to turn on and off the power form the signal drive circuit 21 via the signal line 17 to the pixels (Fig. 1). Akimoto only switches on and off ONE power source, rather switching between TWO power sources: Vs and Vil as the present invention.

Secondly, Applicants respectfully contend that one skilled in the art will not be motivated to combine the teachings in Akimoto and Libsch in the manner suggested by the Examiner. Since Akimoto requires supplying triangular signal amplitude during an illumination period, while Libsch supplying constant signal amplitude during an illumination period, the resulting change in the principle of operation in Akimoto will contradict its intended purpose. It is well established that a rejection based on a principle that contracts the teachings of the cited references is improper. Maintaining Akimoto's principle of operation is much more important than introducing therein the alleged motivation in Libsch (i.e., ensuring the driver transistor Q2 is driven into saturation).

Applicants contend that neither Akimoto, Libsch, nor their combination teaches or suggests each and every feature of the present invention as disclosed in independent claim 1 and at lest the dependent claim 13. As such, the present invention as now claimed is distinguishable and thereby allowable over the rejections raised in the Office Action. The withdrawal of the outstanding prior art rejections is in order, and is respectfully solicited.

Conclusion

In view of all the above, clear and distinct differences as discussed exist between the present invention as now claimed and the prior art reference upon which the rejections in the Office Action rely, Applicants respectfully contend that the prior art references cannot anticipate the present invention or render the present invention obvious. Rather, the present invention as a whole is distinguishable, and thereby allowable over the prior art.

Favorable reconsideration of this application is respectfully solicited. Should there be any outstanding issues requiring discussion that would further the prosecution and allowance of the above-captioned application, the Examiner is invited to contact the Applicants' undersigned representative at the address and phone number indicated below.

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April 8, 2008

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